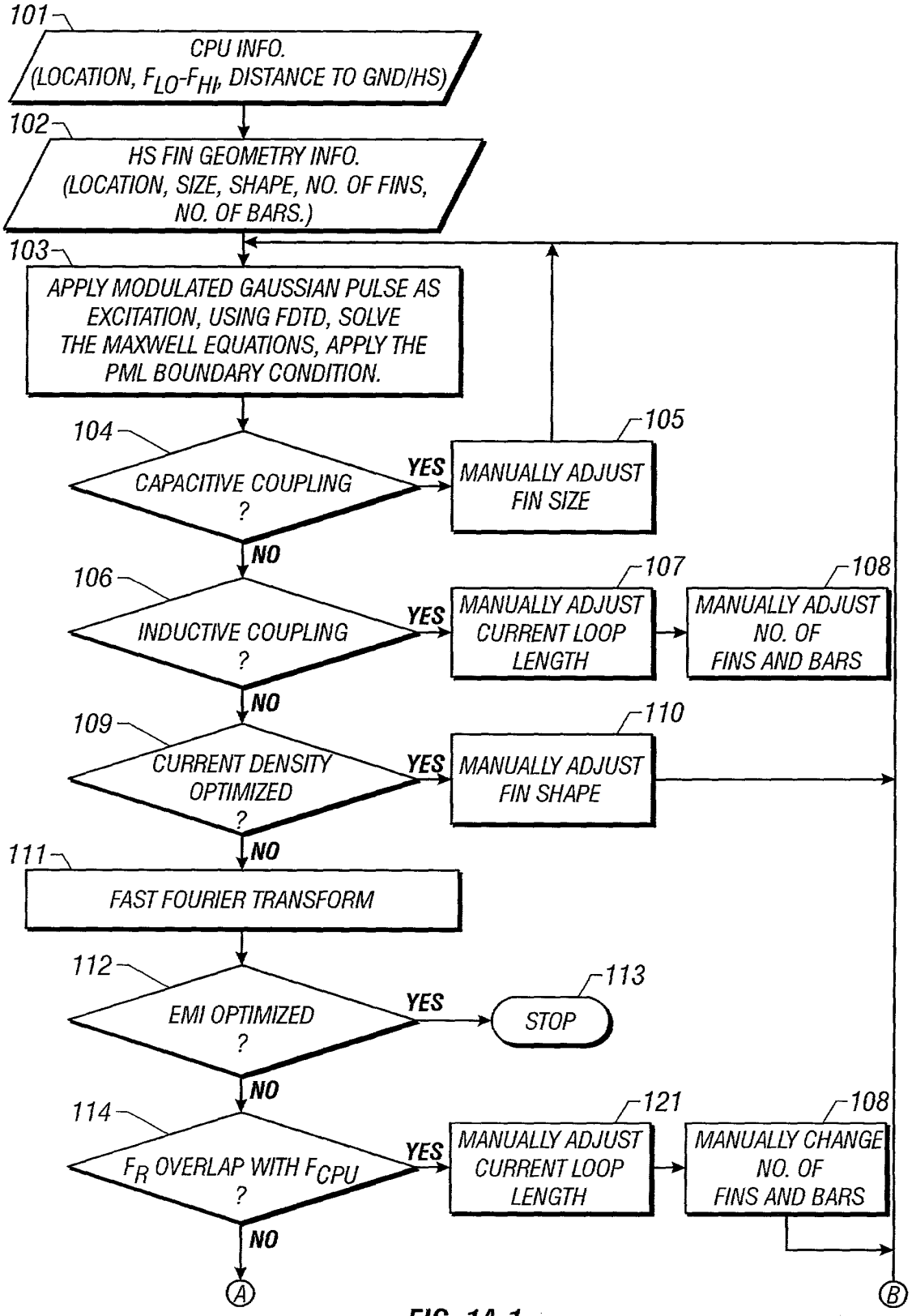
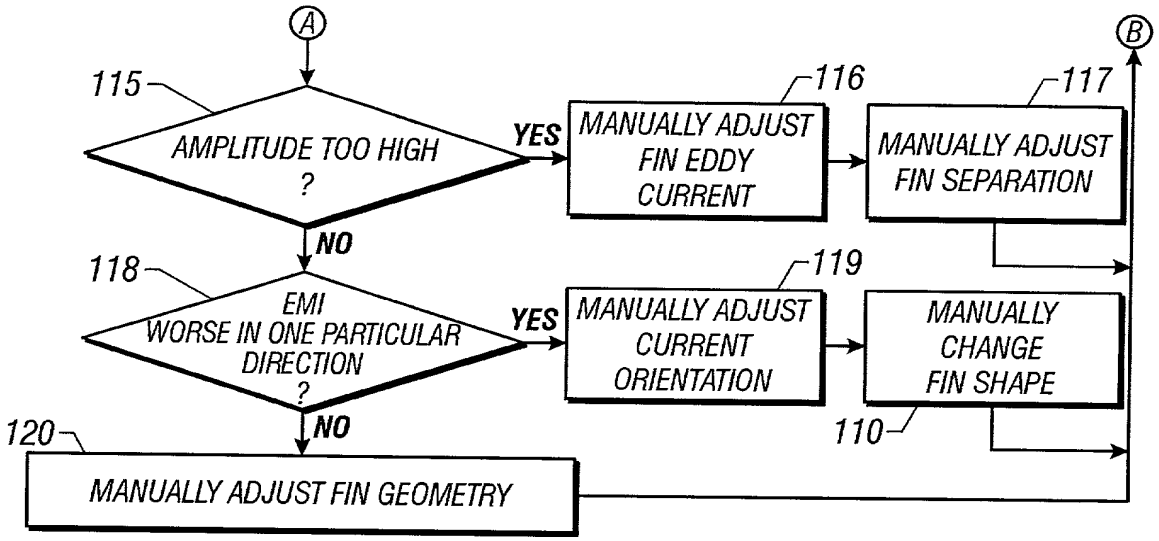

101
CPU INFO.
(LOCATION, F_{LO}-F_{HI}, DISTANCE TO GND/HS)
102
HS FIN GEOMETRY INFO.
(LOCATION, SIZE, SHAPE, NO. OF FINS, NO. OF BARS.)
103
APPLY MODULATED GAUSSIAN PULSE AS EXCITATION, USING FDTD, SOLVE THE MAXWELL EQUATIONS, APPLY THE PML BOUNDARY CONDITION.
104
CAPACITIVE COUPLING ?
YES
105
MANUALLY ADJUST FIN SIZE
NO
106
INDUCTIVE COUPLING ?
YES
107
MANUALLY ADJUST CURRENT LOOP LENGTH
108
MANUALLY ADJUST NO. OF FINS AND BARS
NO
109
CURRENT DENSITY OPTIMIZED ?
YES
110
MANUALLY ADJUST FIN SHAPE
NO
111
FAST FOURIER TRANSFORM
112
EMI OPTIMIZED ?
YES
113
STOP
NO
114
F_R OVERLAP WITH F_{CPU} ?
YES
121
MANUALLY ADJUST CURRENT LOOP LENGTH
108
MANUALLY CHANGE NO. OF FINS AND BARS
NO
A
B

FIG. 1A-1



HS	=HEATSINK
F_{LO}-F_{HI}	=FREQUENCY WINDOW RANGE
F_r	=RESONANCE FREQUENCY OF THE HEATSINK
PML	=PERFECT MATCHED LAYER
FDTD	=FINITE DIFFERENCE IN TIME DOMAIN
GND	=GROUND
FFT	=FAST FOURIER TRANSFORM

FIG. 1A-2

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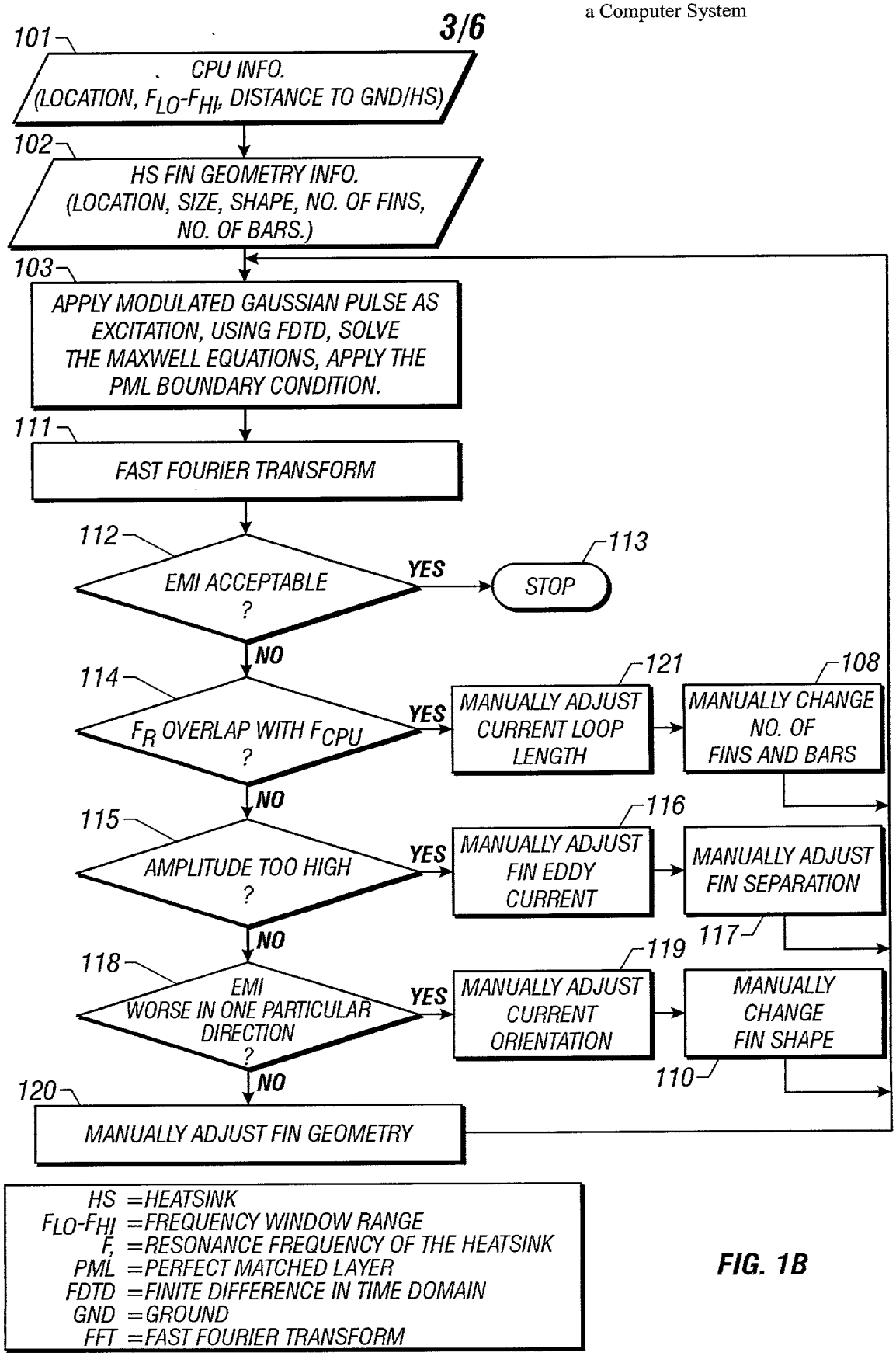

HS =HEATSINK
F_{LO}-F_{HI} =FREQUENCY WINDOW RANGE
F_r =RESONANCE FREQUENCY OF THE HEATSINK
PML =PERFECT MATCHED LAYER
FDTD =FINITE DIFFERENCE IN TIME DOMAIN
GND =GROUND
FFT =FAST FOURIER TRANSFORM

FIG. 1B

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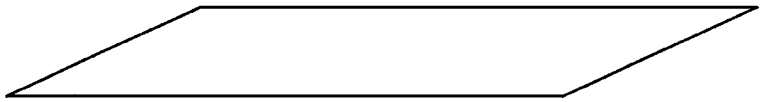
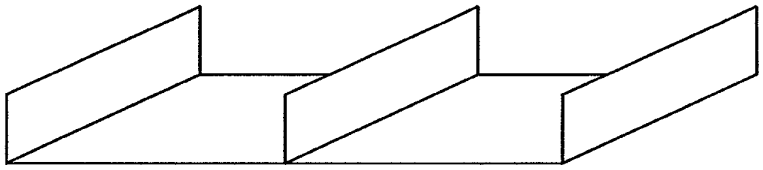


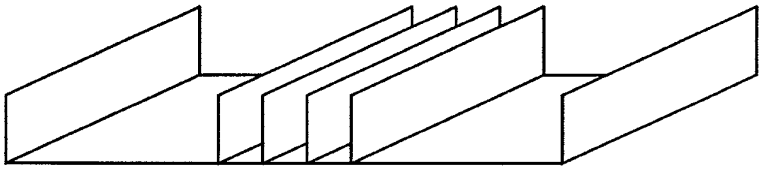
NO FIN, NO TOP

Case A



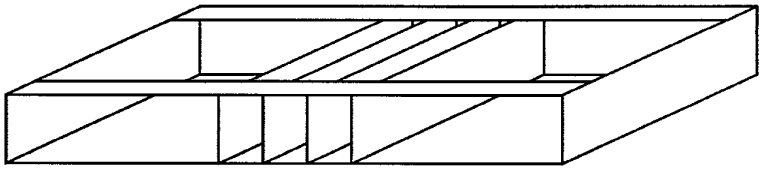
3 FINS, NO TOP

Case B



25 FINS, NO TOP

Case C



25 FINS, 2 TOP BARS

Case D

FIG. 2

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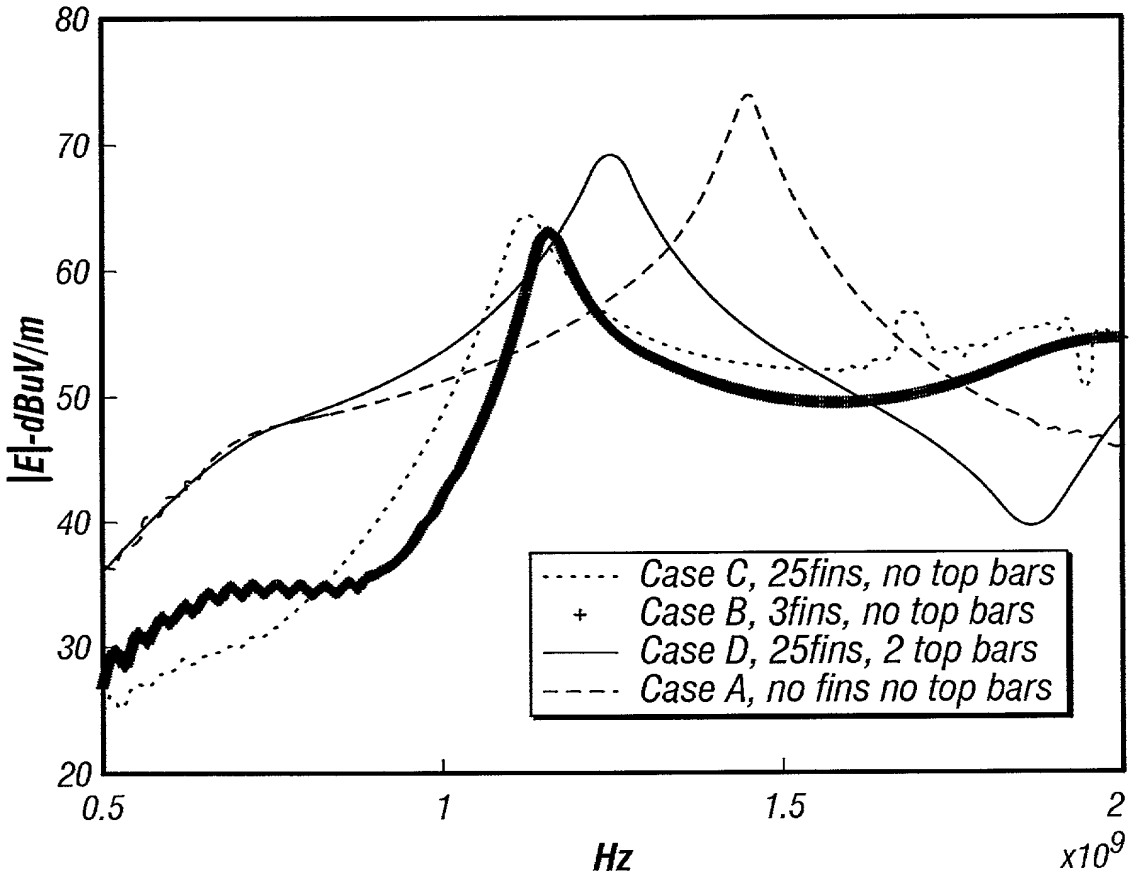
80
70
60
50
40
30
20
|E|-dBuV/m
0.5
1
1.5
2
Hz
x10^9
Case C, 25fins, no top bars
Case B, 3fins, no top bars
Case D, 25fins, 2 top bars
Case A, no fins no top bars

FIG. 3

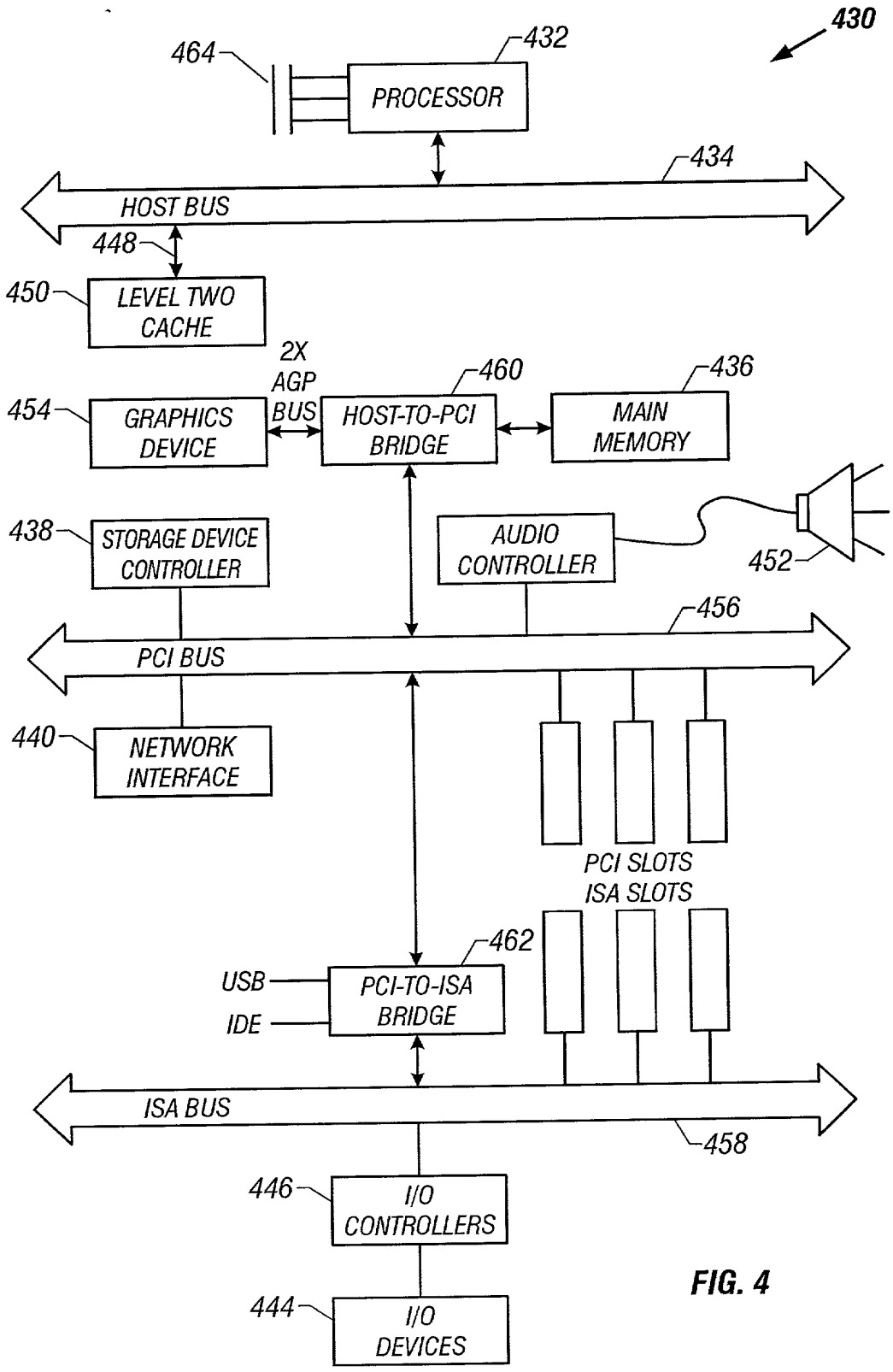
430
464
432
PROCESSOR
434
HOST BUS
448
450
LEVEL TWO CACHE
2X AGP BUS
460
436
454
GRAPHICS DEVICE
HOST-TO-PCI BRIDGE
MAIN MEMORY
438
STORAGE DEVICE CONTROLLER
AUDIO CONTROLLER
452
456
PCI BUS
440
NETWORK INTERFACE
PCI SLOTS
ISA SLOTS
462
USB
IDE
PCI-TO-ISA BRIDGE
ISA BUS
458
446
I/O CONTROLLERS
444
I/O DEVICES

FIG. 4